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(54) Reactive ion etching device

(57) A reactive ion etching device for etching a layer formed on a wafer (8) comprises a first electrode (6) for supporting the wafer (8), and a second electrode (2) opposed to the first electrode (6) with a space therebetween, the space being filled with a reaction gas, between the first electrode (6) and the second electrode (2) there being applied a predetermined power, and is characterized by a material (20, 22, 24, 26) which can reduce the quantity of etching seeds of the reaction gas at substantially the same rate as that of the layer to be etched, and which is disposed at least around the wafer (8) on the first electrode (6). The reactive ion etching device is capable of uniformly etching the semiconductor wafer or the layer thereon.

FIG. 3

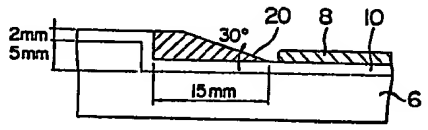

FIG. 5

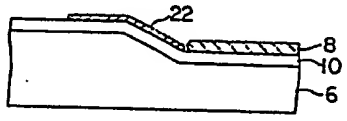

FIG. 6

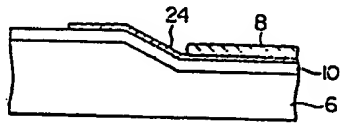

FIG. 7

FIG. 8

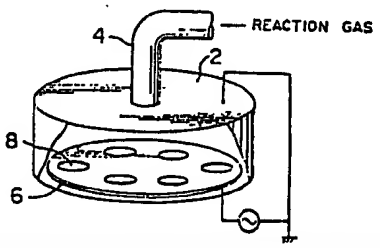

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FIG. 1(a)

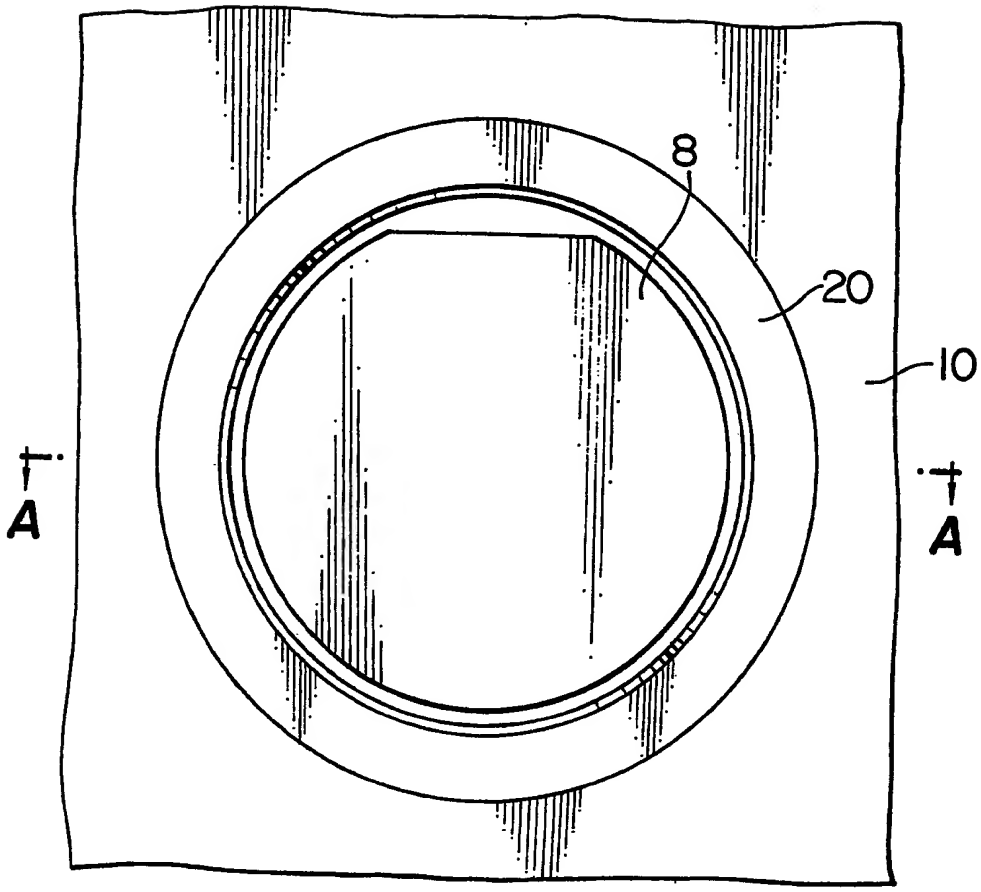


FIG. 1(b)

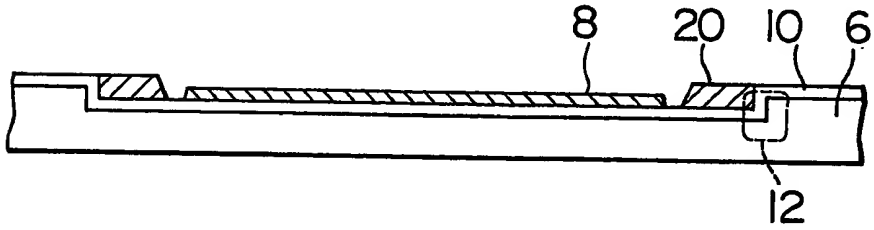
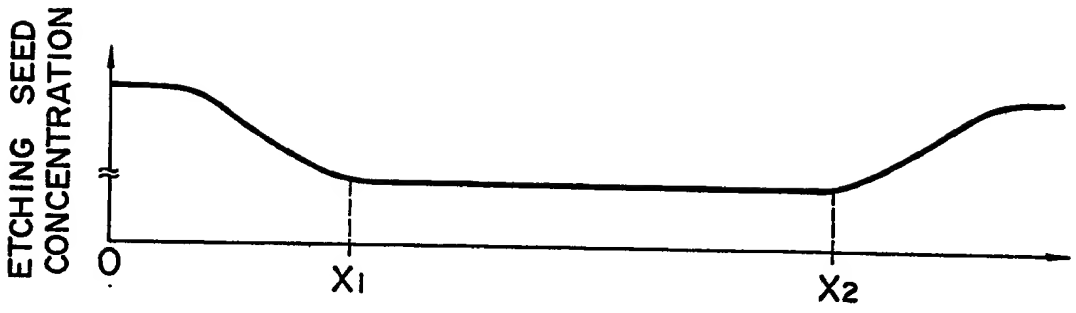


FIG. 2



COORDINATES IN THE DIAMETRICAL DIRECTION OF A WAFER

FIG. 3

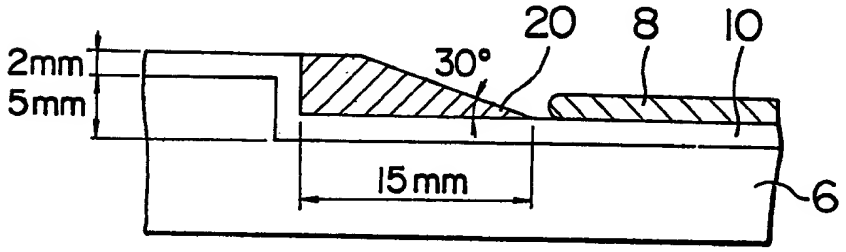
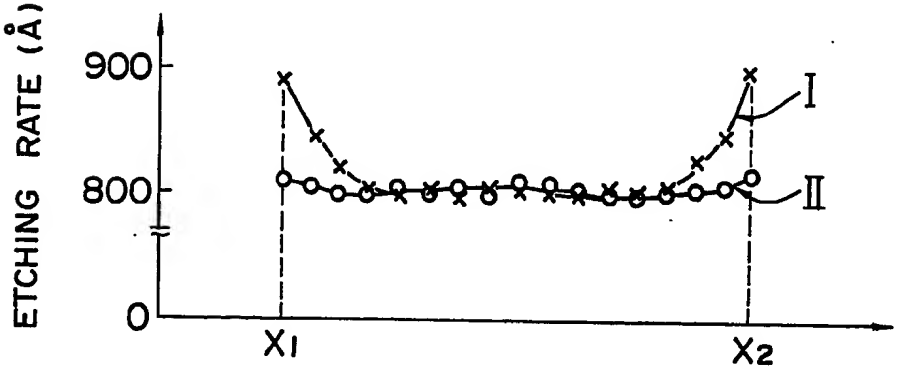


FIG. 4



COORDINATES IN THE DIAMETRICAL DIRECTION OF A WAFER

FIG. 5

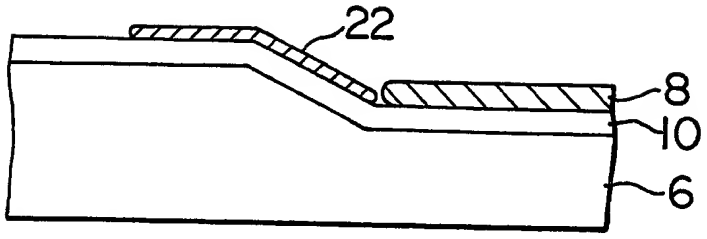


FIG. 6

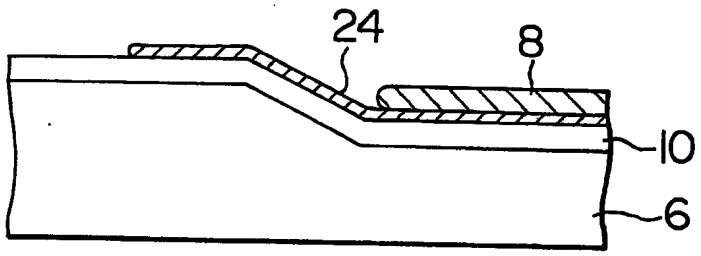


FIG. 7

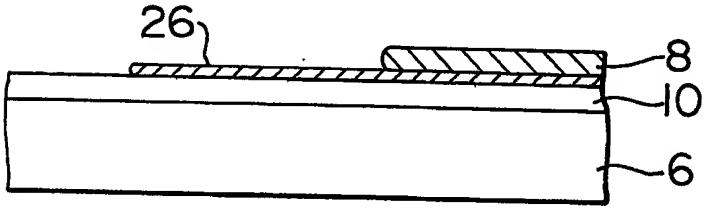


FIG. 8

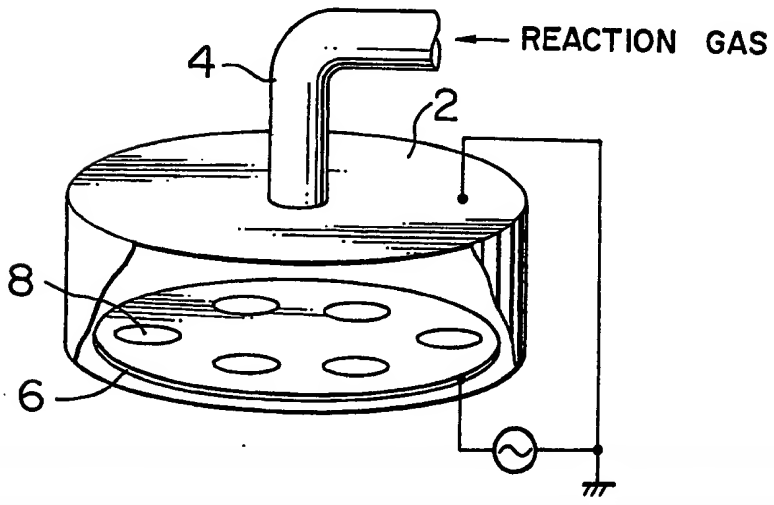


FIG. 9

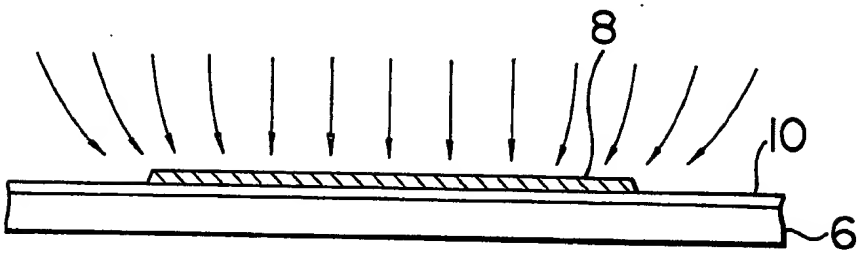


FIG. 10

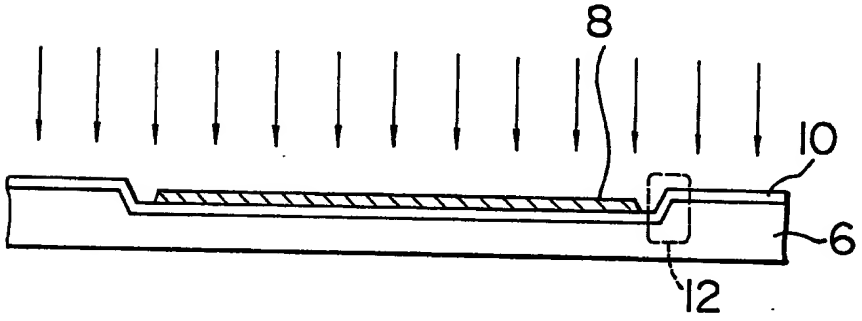


FIG. 11

SPECIFICATION

Reactive ion etching device

Background of the invention

The present invention relates to a reactive ion etching device for etching a semiconductor wafer or a layer formed thereon.

Figure 8 shows a reactive ion etching device whose top is connected to a reactive gas introduction pipe 4 for introducing a reactive gas into an etching chamber 2 in which an electrode 6 is disposed. A plurality of semiconductor wafers 8 are mounted on the electrode 6. In an etching process carried out in such reactive ion etching device, the etching chamber 2 is evacuated by means of a vacuum pump (not shown), and a reaction gas is introduced into the etching chamber 2 through the introduction pipe 4. The etching chamber 2 functions as an upper electrode and is grounded. When a predetermined power is applied between the etching chamber 2 and the electrode 6, a layer on the semiconductor wafers 8 is etched physically or chemically.

Figure 9 shows in cross section the wafer mounting portions of the electrode 6 of the prior art etching device. As shown in Figure 9, the semiconductor wafers 8 are mounted on an insulating plate 10 mounted on the flat electrode 6. Electric fields are concentrated around the semiconductor wafers 8 as shown in Figure 9 because the semiconductor wafers 8 themselves have some thickness. As a result, there arises the problem that etching rate becomes faster at the peripheral portions of the semiconductor wafers 8, so that the top major surface thereof is not etched uniformly.

In order to compensate such electric field concentrations described above, there has been proposed an assembly of an electrode 6 and an insulating plate 10 for physical etching which, as shown in Figure 10, is so designed and constructed that a semiconductor wafer 8 may be located at a lower position. More particularly, a portion of the electrode 6 is recessed as indicated by 12 so that the top surface of the semiconductor wafer 8 mounted on the top surface of the electrode 6 is slightly lower than the top surface of the insulating plate 10. As a result, the undesired electric field concentrations around the semiconductor wafers 8 can be eliminated, and therefore a uniform electric field distribution can be attained. Then uniform etching can be enhanced.

When the etching process is caused to proceed by a physical reaction; that is, the upper surface of the semiconductor wafer 8 is physically etched by the bombardments of ions and radicals of the reaction gas on the upper surface of the semiconductor wafer 8, uniform etching may be ensured by a uniform electric field distribution. In the case, however, where the etching process is mainly carried out by chemical reactions, the etching seeds (i.e., the ions and radicals which directly participate in the chemical reactions) in the reaction gas affect the etching depending upon their distribution.

For instance, in the case of etching aluminum, the etching process is dominantly carried out by the reactions expressed by the following chemical equations:

$$Al + 3Cl^* \rightarrow AlCl_3^* \uparrow \text{ and}$$

$$Al + SiCl_3+ \rightarrow AlCl_3 \uparrow + Si.$$

Therefore, if a distribution of etching seeds such as Cl^* and Cl^+ is not uniform, then the etching rate will not be uniform.

In the case where the aluminum etching is carried out in the reactive ion etching device of the type as shown in Figure 10 which has the electrode 6, a uniform electric field distribution as well as a uniform reaction gas distribution can be attained, so that uniform etching is ensured at the initial stage. But as the etching process proceeds, the reactions reduce the etching seeds in number immediately above the semiconductor wafer 8. The reduction of the etching seeds is almost negligible around the peripheral portion at which none of the semiconductor wafer exists. As a result, as shown in Figure 11, the closer to the periphery of the semiconductor wafer 8, the higher the concentration of the etching seeds becomes. Since the etching rate distribution is dependent on an etching seed distribution, there arises the problem that uniform etching cannot be ensured.

Summary of the Invention

An object of the present invention is to provide a reactive ion etching device which is capable of uniformly etching a semiconductor wafer or a layer thereon.

The above object can be realized by a reactive ion etching device for etching a layer formed on a wafer, comprising a first electrode for supporting said wafer, and a second electrode opposed to said first electrode with a space therebetween, said space being filled with a reaction gas, between said first electrode and said second electrode there being applied a predetermined voltage, characterized by a material which can reduce the quantity of etching seeds of said reaction gas at substantially the same rate as that of said layer to be etched, and which is disposed at least around said wafer on said first electrode.

Brief description of the drawings

Figures 1(a) and *(b)* are a plane and cross-sectional views illustrating respectively a wafer mounting portion of an electrode of a reactive ion etching device according to a preferred embodiment of the present invention;

Figure 2 is a graph illustrating an etching seed distribution attained in the reactive ion etching device as shown in Figures 1(a) and (b);

Figure 3 is a view illustrating an optimum geometry of the wafer mounting portion;

Figure 4 is a graph illustrating an etching rate distribution when the wafer mounting portion has the optimum geometry and an etching rate distribution of the prior art reactive ion etching device;

Figures 5, 6 and *7* show variations, respectively, of the wafer mounting portion;

Figure 8 is a schematic view of a reactive ion etching device;

Figures 9 and *10* are views illustrating the shape of the wafer mounting portions, respectively, of an electrode used in the prior art reactive ion etching device; and

Figure 11 is a graph illustrating an etching seed concentration attained in the prior art reactive ion etching device.

Detailed description of the invention

Figure 1 shows a wafer mounting portion of a reactive ion etching device in accordance with one embodiment of the present invention. One of the most important features of this embodiment resides in the fact that an etching correction ring 20 is disposed around a semiconductor wafer 8. More particularly, the recessed portion of an electrode 6 and an insulating plate 10 are greater in diameter than the semiconductor wafer 8 and the correction ring 20 is disposed between the semiconductor wafer 8 and a stepped portion 12, or the peripheral wall of the recess.

The material of the correction ring 20 is dependent on a layer to be etched and may be one which reduces the quantity of the etching seeds of a reaction gas at substantially the same rate as a layer to be etched, in other words, the etching rate of the layer to be etched is substantially equal to that of the correction ring. Specifically, it is preferable that the correction ring 20 has the major part made of the same material as that of the layer to be etched. More preferably the whole correction ring 20 is made of the same material as that of the layer to be etched. In other words, this condition is satisfied if the etching rates of the layer to be etched and of the correction ring 20 are substantially equal to each other.

For instance, where the layer to be etched is an aluminum layer, it is preferable that the correction ring 20 is made of (1) aluminum (Al), (2) a material whose major component is aluminum, (3) titanium-tungsten (TiW), or (4) a material whose major component is titanium-tungsten. If the layer to be etched is a Silicide ($MoSi_2$) layer, it is preferable that the correction ring 20 is made of (1) Molybdenum Silicide ($MoSi_2$), (2) a material whose major component is Molybdenum Silicide ($MoSi_2$), (3) Silicon (Si), or (4) a material whose major component is Silicon (Si).

As described above, according to the present embodiment, the material which can reduce the quantity of the etching seeds at substantially the same rate as that of the semiconductor wafer is disposed around the semiconductor wafer, so that, as shown in Figure 2, a uniform distribution of etching seeds can be obtained over the upper surface of the semiconductor wafer 8. As a result, the semiconductor wafer can be uniformly etched.

The shape of the correction ring 20 is also dependent upon the configuration of an etching chamber and the distance between a pair of electrodes, so that it cannot be specified. In laboratorial experiments, however, optimum effect could be obtained where the layer to be etched was made of aluminum and the correction ring was made of pure aluminum (99.995%) and had a cross sectional geometry as shown in Figure 3, i.e. the recess formed in the upper surface of the electrode 6 was 5 mm in depth, the insulating plate 10 was 2 mm in thickness, and the correction ring 20 was 15 mm in width and 5 mm in thickness and was tapered downwardly by 30° toward the periphery of the semiconductor wafer 8. In this case, the etching rate is distributed as indicted by the curve II in Figure 4. It is seen from the curve that the etching rate is uniform over the upper surface of the wafer. In the case where the prior art reactive ion etching device was used, the difference in etching rate (curve I in Figure 4) between the center portion and the peripheral portion of the wafer was higher than 10%. But it is seen from the curve II that variations in etching rate are of the order of 2.4% The data shown in Figure 4 were obtained by use of a parallel-plate type cathode-coupled reactive ion etching device in which $SiCl_4$, a reaction gas, was made to flow at a rate of 100SCCM, under the etching pressure of 100 mTorr and with RF power of 700W. The etched semiconductor wafer was obtained by forming an aluminum layer (Al-2%Si layer) of 1.0 μm - thickness by a conventional sputtering process over a thermally oxidized film of 5000Å - thickness on a single crystal silicon substrate. In the case of the etching process, a photo resist was used as a mask and the patterning process was accomplished by a conventional photolithographic process.

Figures 5, 6 and 7 show variations of the electrode used in the reactive ion etching device in accordance with the present invention. In Figure 5, the peripheral wall of the recess formed in the electrode 6 and in the insulating plate 10 is tapered, and an etching correction film 22 is formed by a sputtering process around the semiconductor wafer 8. The material of the etching correction film 22 is the same as the correction ring. The function of the correction film 22 is substantially similar to that of the correction ring of the type described above so that a uniform etching seed distribution and thus uniform etching can be ensured. While in Figure 5 the correction film 22 is not extended below the semiconductor wafer 8, a correction film 24 may be extended under the semiconductor wafer 8 as shown in Figure 6. Alternatively, the recess is not necessary in the upper surface of the electrode 6, and, as shown in Figure 7 a correction film 26 may be formed on the insulating plate 10. The same effect as described above can be attained.

If the reaction gas introduction pipe 4 is connected only at the center of the top of the etching chamber as shown in Figure 8, all the wafers placed in the etching chamber are not uniformly etched. This problem can be simply solved by connecting individual reaction gas introduction pipes to the etching chamber immediately above the respective wafers.

It is to be understood that the reactive ion etching device in accordance with the present invention can etch not only layers on single-crystal silicon substrates but also layers on Ga-As single-crystal substrates.

CLAIMS

1. In a reactive ion etching device for etching a layer formed on a wafer, comprising a first electrode for supporting said wafer, and a second electrode opposed to said first electrode with a space therebetween, said space being filled with a reaction gas, between said first electrode and said second electrode there being applied a predetermined power, the improvement which comprises a material which can reduce the quantity of etching seeds of said reaction gas at substantially the same rate as that of said layer to be etched, and which is disposed at least around said wafer on said first electrode.

2. A reactive ion etching device according to Claim 1, wherein a portion of said first electrode on which said wafer is mounted in recessed so that an electric field distribution between said first electrode and said second electrode can be uniform.

3. A reactive ion etching device according to Claim 1 or 2, wherein a correction ring made of said material is disposed on said first electrode around said wafer.

4. A reactive ion etching device according to Claim 3, wherein the thickness of said correction ring becomes gradually thin toward the periphery of said wafer.

5. A reactive ion etching device according to Claim 1 or 2, wherein said material is deposited on said first electrode around said wafer.

6. A reactive ion etching device according to Claim 5, wherein said material is deposited on said first electrode under said wafer.

7. A reactive ion etching device according to any one of Claims 1 to 6, wherein the etching rate of said material is substantially equal to that of said layer to be etched.

8. A reactive ion etching device according to Claim 7, wherein a main portion of said material is the same material as said layer to be etched.

9. A reactive ion etching device according to Claim 7, wherein said material is the same material as said layer to be etched.

10. A reactive ion etching device substantially as hereinbefore described with reference to Figures 1*a* to 3 or these figures as modified by one of the Figures 5 to 7 of the accompanying drawings.

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